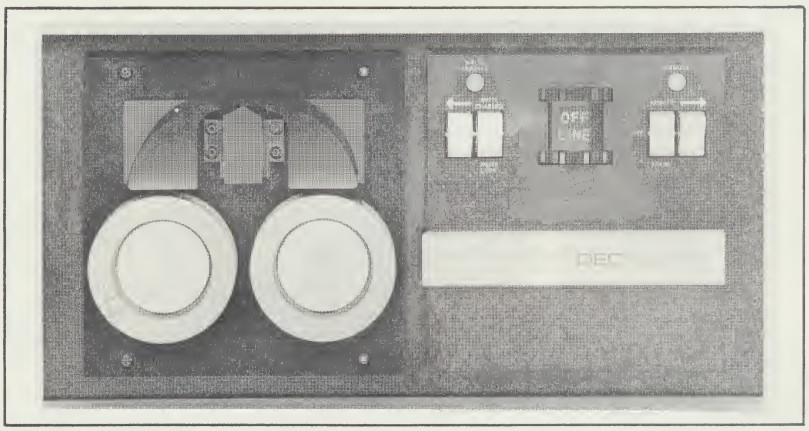
DIGITAL

DECTAPE TRANSPORT TYPE TU55



The TU55 is a bidirectional magnetic-tape transport designed and manufactured by DEC for use with PDP-7 and PDP-8 general-purpose computers. The device consists of a read/write head for recording and playback of information on five channels of the tape, each channel consisting of two nonadjacent tracks with windings connected in series to provide exceptionally high reliability (less than one transient error in 10^{10} characters). Specific functions performed by each of these channels and the format of information depends upon the control unit used with the TU55. Connections from the read/write head are made directly to the external control which contains the read and write amplifiers. The DECtape controls used with the TU55 are the Types 550 and 550B used with the PDP-4 and PDP-7, and the Types 552 and 552B used with the PDP-5 and PDP-8.

During normal data reading with the PDP-8, for example, the 552 Control assembles 12-bit computer length words from four successive lines read from the information channels of the tape. During normal data writing, the control disassembles 12-bit words and distributes the bits so they are recorded on four successive lines on the information channels. A mark channel error check circuit assures that one of the permissable marks is read in every six lines on the tape. This 6-line mark channel sensing requires that data be recorded in 12-line segments (12 being the lowest common multiple of 6-line marks and 4-line data words) which correspond to three 12-bit words.

A tape contains a series of data blocks that can be of any length which is a multiple of three 12-bit words. Block length is determined by information on the mark channel. Usually a uniform block length is established over the entire length of a reel of tape by a program which writes mark and timing information at specific locations. The ability to write variable-length blocks is useful for certain data formats. For example, small blocks containing index or tag information can be alternated with large blocks of data. (Software supplied with DECtape allows writing for fixed block lengths only.)

Between the blocks of data are areas called interblock zones. The interblock zones consist of 30 lines on tape before and after a block of data. Each of these 30 lines is divided into five 6-line control words. These 6-line control words allow compatibility between DECtape written on any of DEC's 12-, 18-, or 36-bit computers. As used on the PDP-8, only the last four lines of each control word are used.

The logic circuits of the TU55 control tape movement in either direction over the read/write heads. Tape drive motor control is exercised completely through the use of solid state switching circuits to provide fast reliable operation. These switching circuits contain silicon controlled rectifiers (SCR) which are controlled by normal DEC diode and transistor logic circuits. The function of these circuits is simply to control the torque of the two motors which transport the tape across the head according to the established function of the device, i.e., go, forward, reverse, or stop. In normal tape movement, full torque is applied to the forward or leading motor and a reduced torque is applied to the reverse or trailing motor to keep proper tension on the

tape. Since tape motion is bidirectional, each motor serves as either the leading or trailing drive for the tape, depending upon the forward or reverse control status of the TU55. A positive stop is achieved by an electromagnetic brake mounted on each motor shaft. When a stop command is given, the trailing motor brake latches to stop tape motion. Enough torque is then applied to the leading motor to take up slack in the tape.

Tape movement can be controlled by commands originating in a computer and applied to the TU55 via a suitable DECtape control, or can be controlled by commands generated by manual operation of rocker type switches located on the front panel of the transport. Manual control is used to mount new reels of tape on the TU55, or as a quick maintenance check for proper operation of the control logic in moving the tape.

The solid state TU55 is completed compatible with the older Type 555 Dual DECtape Transport and may be used to expand systems using the Type 555 Transport.

SPECIFICATIONS

General

Overall Size - 10-1/2 in. high, 19-1/2 in. wide, 9-3/4 in. deep

Mounting - Standard 19 in. rack. Four #10 32 screws mount chassis track assembly which holds transport. Chassis can be extended 16-3/4 in. beyond mounting surface for maintenance.

Power Requirements - −15 vdc, 10 amp maximum, +10 vdc, 50 ma maximum, 115 vac ±10%, 1.0 amp idle, and 2.0 amp maximum current (60-cps models standard, 50-cps models on request

Connectors - Commands: two 18-terminal FLIP CHIP female connectors. Information: two 36-terminal FLIP CHIP female connectors

Cooling - Internally mounted fan is provided

Operating Temperature - 50°F to 100°F ambient

Humidity - 10 to 90% relative humidity

NOTE: The manufacturer of the magnetic tape for DECtape recommends 40 to 60% relative humidity and 60°to 80°F as acceptable for operating environment.

Tape Characteristics

Capacity - 260 ft of 3/4 in., 1 mil Mylar sandwich tape

Reel Diameter - 2.8 in. empty reel, 3.9 in. for 260 ft of tape

Reel Diameter Ratio - 1:4 (maximum to minimum)

Tape Handling - Direct drive hubs and specially designed guides which float the tape over the head hydrodynamically. No capstans or pinch rollers are used.

Speed - 97 ± 14 ips

Density - 350 ± 55 bpi

Information Capacity - 2.7×10^6 bits per reel assembled into computer-length words by external DECtape control

Tape Motion - Bidirectional

Drive Characteristics

Times given are for 90% full speed.

Start Time - <200 msec

Stop Time - <150 msec

Turn Around Time - <200 msec

Input Signals to Transport from Control

Commands* - FORWARD (ground level assertion), REVERSE (ground level assertion), GO (ground level assertion), STOP (ground level assertion), and ALL HALT (negative level assertion) used to stop transport when computer halts.

Unit Select* - SELECT 1 through SELECT 8 (ground level assertion)

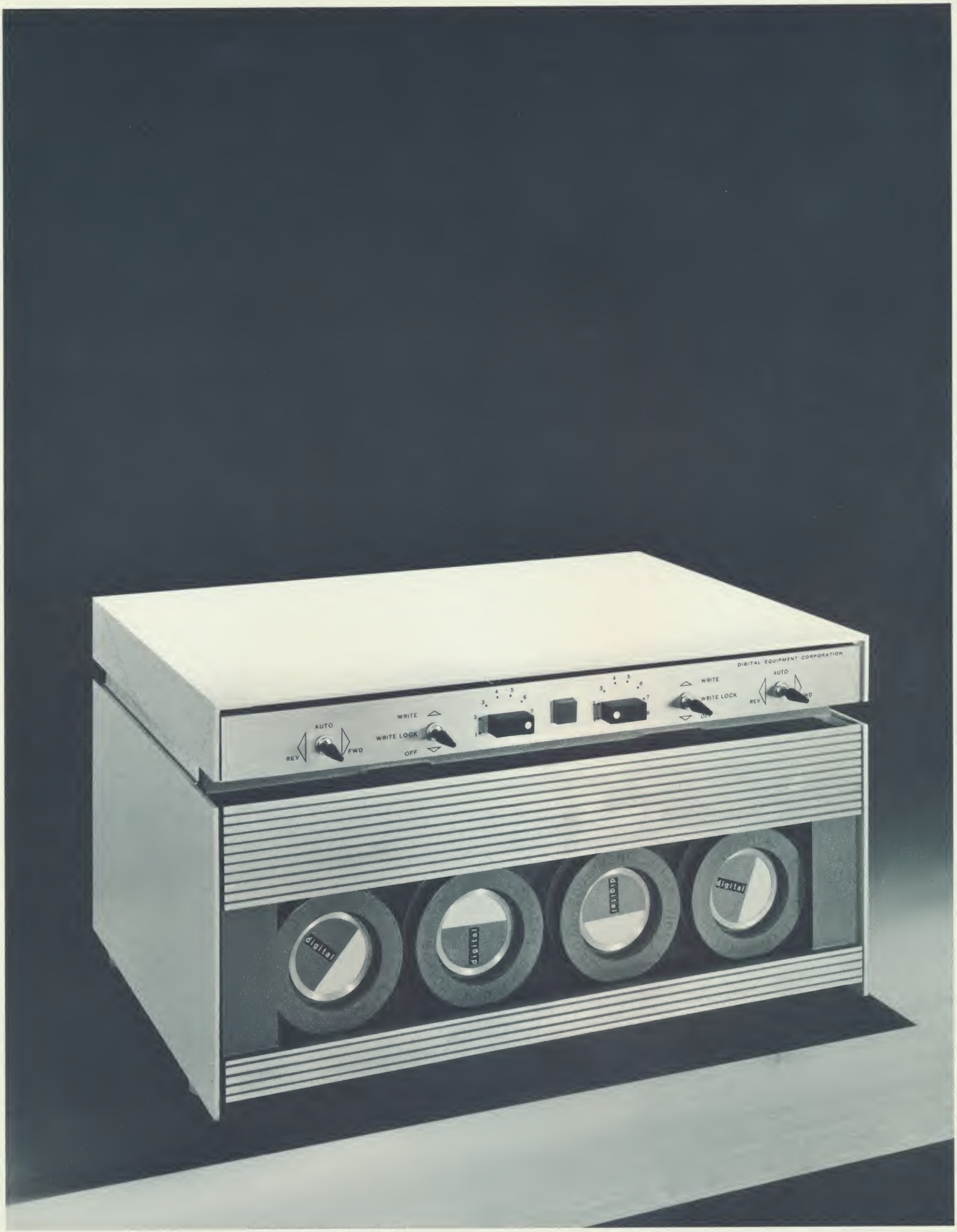
Control - POWER CLEAR standard DEC negative pulse to clear MOTION flip-flop when computer power is turned on

Output Signal from Transport to Control

Control - WRITE ENABLE standard DEC ground level for assertion

Price $2,350

*These signals are approximately −3v and −15v when supplied by a control unit designed to operate the Type 555 Dual DECtape Transport which uses relay switching logic circuits, or are standard DEC logic levels of ground and −3v when supplied by a control unit designed specifically to drive the TU55.



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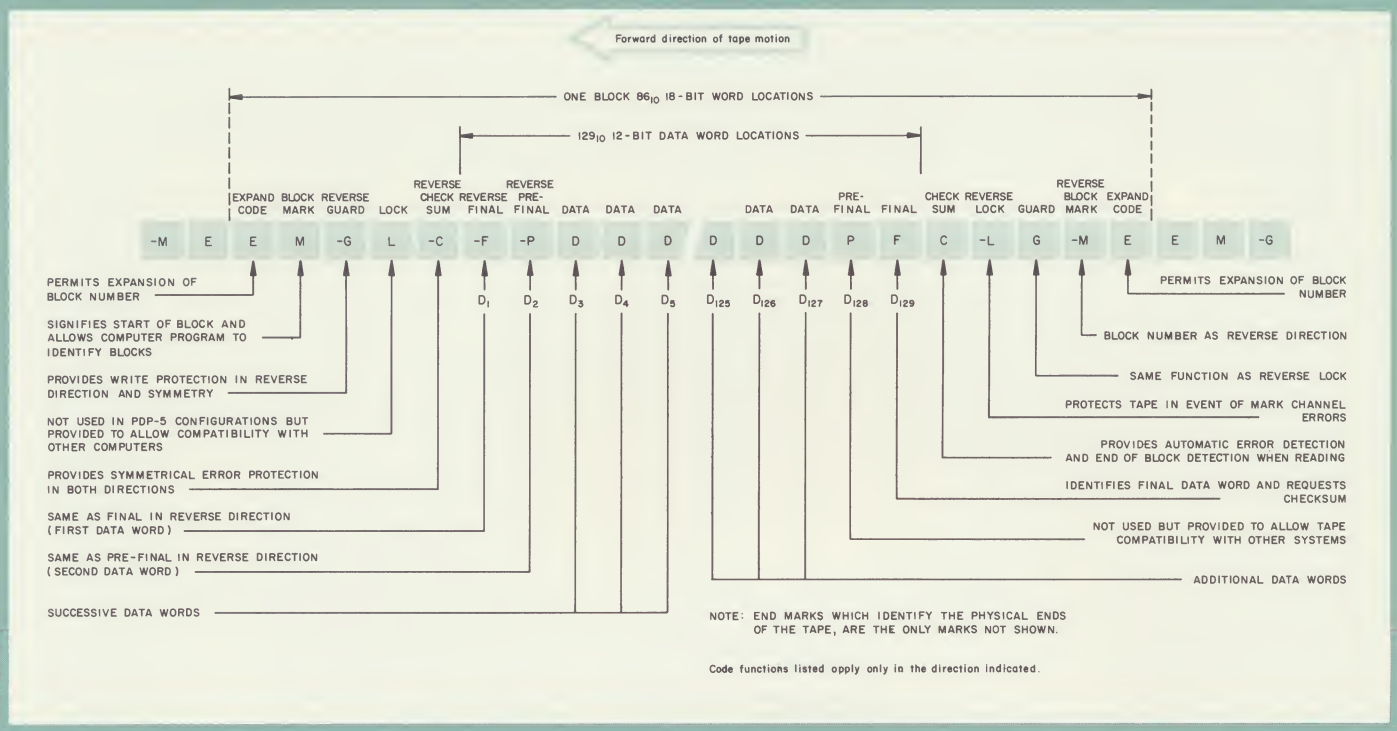


Figure 2. DECtape Mark Channel Format (Assumes 129_{10}, 12-bit Data Word Locations Per Block)

Figure 3. Control and Data Word Assignments

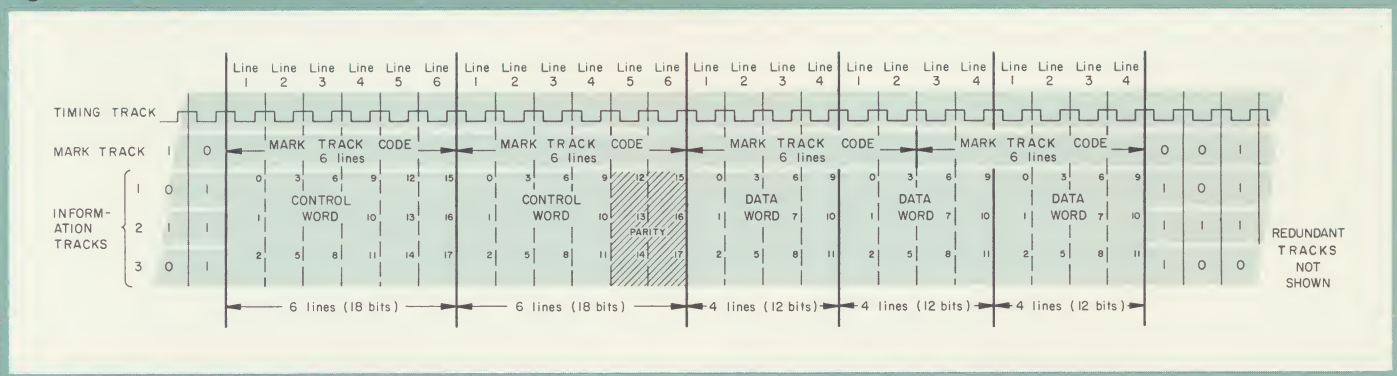


Figure 4. Basic Tape Units — Data and Control Words

FUNCTIONAL UNITS

The basic functional elements of the 552 control and the 555 transport are shown in the block diagram as they interface with the PDP-5/8. The main functional elements of the system are:

Data Buffer (DB): This 12-bit register serves as a storage buffer for data to be transferred between DECtape and the computer memory buffer register. During a read operation information sensed from the tape is transferred into the DB from the read/write buffer and is transferred to the computer during a data break cycle. During a write operation the DB receives information from the computer and transfers it to the read/write buffer for disassembly and recording on tape. In this manner the DB synchronizes data transfers by allowing transfers between itself and the read/write buffer as a function of the tape timing.

Read/Write Buffer (R/WB): This 12-bit register is composed of three 4-bit shift registers. During reading, one bit from each information channel is read into a separate segment of the R/WB and shifted right or left as a function of the direction of tape movement. When four tape positions have been read, the content of the R/WB is set into the DB as an assembled 12-bit computer word. During writing, the contents of each segment of the R/WB is shifted serially to the write register (one bit from each of the three segments of the R/WB is transferred into the write register at a time to provide the data to be written at one line) for recording on tape.

Write Register: A 3-bit register which is alternately loaded from the R/WB and complemented to write the phase-coded information on tape.

Select Register: This 4-bit register is loaded under program control to specify the tape drive selected for operation from the control unit. A single Type 522 DECtape Control can select the drives of four Type 555 Dual DECtape Transports (eight tape drives).

Motion Register: This 2-bit register contains a go/stop flip-flop and a forward/reverse flip-flop which control the motion of the selected tape drive. The register is set under program control.

Longitudinal Parity Buffer (LPB): This 6-bit register performs a parity check of the information in the three information channels. The check essentially reads the number of binary zeros in each half of a 12-bit data word and forms a parity bit to be recorded in the checksum control word at the end of the data block. This is effected by setting the information read from two consecutive tape positions into the LPB and then complementing a bit of the LPB if the corresponding bit of the R/WB contains a 0. After reading a block of data the LPB holds a number which indicates the parity of bits 0 and 6, 1 and 7, etc. A 1 in the LPB at this time indicates odd parity and a 0 indicates even parity. This information is compared with the data stored in the checksum control word during reading and is used to generate the checksum during writing. If the data read is not equal to the checksum the parity or mark channel error flip-flop is set to 1.

Memory Address Counter (MAC): This 12-bit register specifies an address in computer core memory to be used for each word transfer. During program initialization, the starting address of a transfer is set into MAC from the computer accumulator. During the transfer, the address contained in MAC is transferred into the computer memory address register for each data word. The contents of MAC is incremented by 1 at the conclusion of each word transfer so that transfers occur between successive addresses of computer core memory and tape, regardless of tape direction.

Window (W): This 9-bit register serves as a control signal generator for the DECtape system. The mark channel data is stored in the W and control signals are generated as a function of the mode of operation in progress and the contents of the W. For example, in the search mode when the W detects a block mark, control signals are generated to raise the DECtape (DT) flag to indicate the presence of a block number in the DB and signals the start of data block to the computer.

Device Selector (DS): The device selector is a gating circuit which produces the IOT pulses necessary to initiate operation of the DECtape system and strobe information into the computer.

Dectape Flag (DT): This flip-flop serves as an indicator of DECtape system operation to the computer and is connected to the computer program interrupt facility. The function of the DT flag is determined by the control mode in operation at the time, as follows:

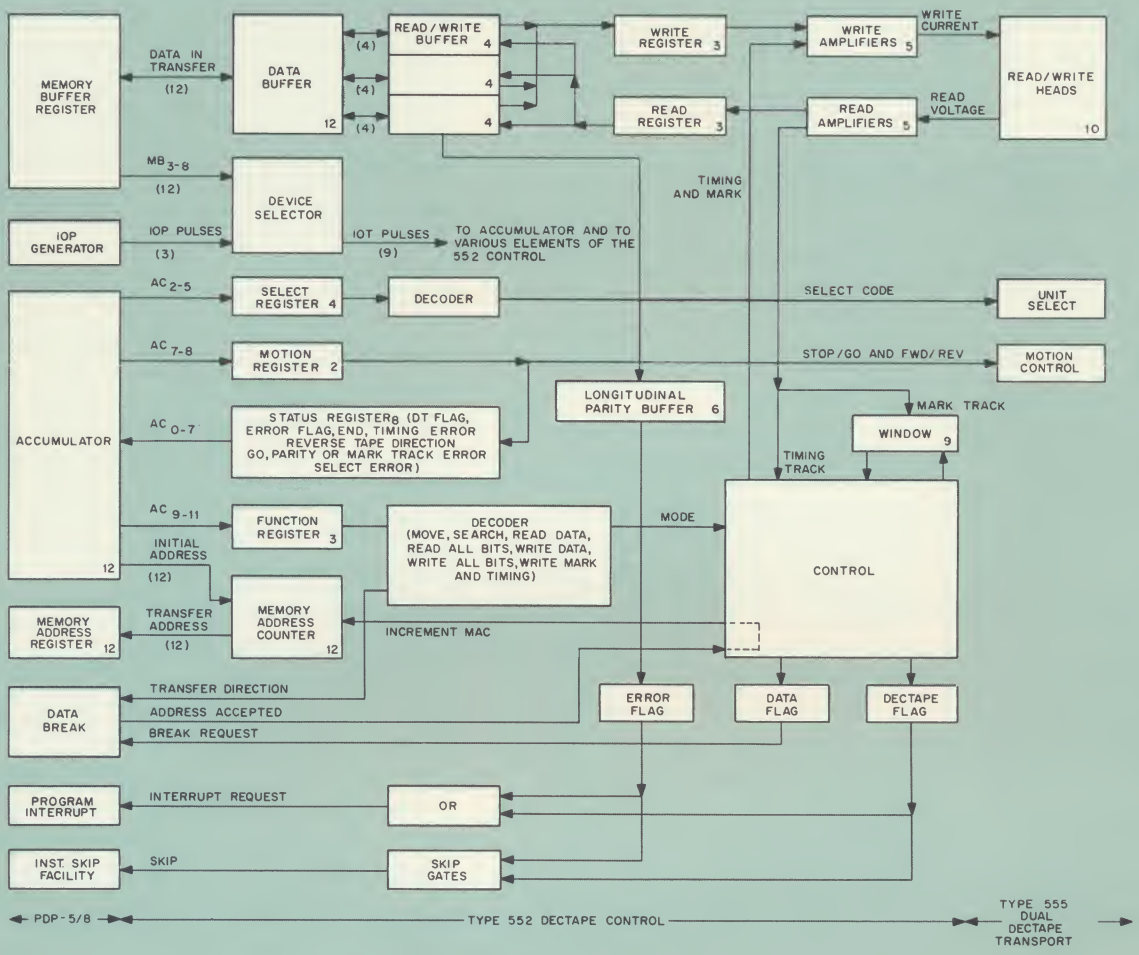
a. In the search mode the DT flag rises each time a block mark (block number) is read to indicate the beginning of a new block and to allow proprammed determination of the block number which just passed the read/write head.

b. In the read data or write modes the DT flag rises at the end of each block to indicate the end of a data block. Under these conditions the computer program can sense for this flag to determine when the transfer is complete.

c. In the read all bits or write all bits modes the DT flag rises to indicate completion of each 12-bit word transfer. Since block marks are not observed in these modes, this flag can be used by the computer program to count the number of words transferred as a means of determining tape location.

Error Flag: This flag is raised by four error conditions. When the flag rises it initiates a program interrupt to allow the computer interrupt subroutine to determine the condition of the 552 control by means of a read status command. The four error conditions indicated are:

a. *End:* The tape of the selected transport is in the end zone and tape motion is stopped automati-



DECtape SYSTEM BLOCK DIAGRAM AND PDP-5/8 INTERFACE

cally. Under these conditions end is an error if it is not expected by the program in process or is a legitimate signal used to indicate the end of a normal operation (such as rewind) if it is anticipated by the program. If the transport is not selected when the tape enters the end zone this signal is not given, tape motion is not stopped automatically, and the tape can run off the end of the reel.

b. *Timing Error:* The program was not able to keep pace with the tape transfer rate or a new motion or select command was issued before the previous command was completely executed.

c. *Parity or Mark Track Error:* Indicates that during the course of the previous block transfer a data parity error was detected, or one or more bits have been picked up or dropped out from either the timing track or the mark track.

d. *Select Error:* Signifies that a tape transport unit select error has occurred such that more than one transport in the system have been assigned the same select code or that no transport has been assigned the programmed select code.

Therefore, a select error indicates an error by the operator, a timing error is a program error, and a parity or mark track error indicates an equipment malfunction. Under certain conditions the end may also be an indication of equipment malfunction.

Data Flag: This flag is raised each time the DECtape system is ready to transfer a 12-bit word with the computer. When raised, the flag produces a computer data break.

DECtape INSTRUCTION LIST

MNEMONIC	OCTAL	OPERATION
MMLS	6751	Load unit select register from the content of AC 2-5 and clear DECtape (DT) flag. DT flag is automatically set approximately 70 msec. after this IOT.
MMLM	6752	Load motion register from the content of AC 7-8 and clear DT flag. DT flag is automatically set approximately 70 msec. after this IOT.
MMLF	6754	Load function register from the content of AC 9-11, then clear the AC. The octal code of these three bits establishes the following DECtape control modes: 0 = Move 1 = Search 2 = Read data 3 = Read all bits 4 = Write data 5 = Write all bits 6 = Write mark and timing
MMSF	6761	Skip if DT flag is a 1.
MMCC	6762	Clear memory address counter (MAC).
MMLC	6764	Load MAC from the content of AC 0-11 and then clear the AC. (One's transfer).
MMML	6766	Clear and load MAC from the content of AC 0-11 and then clear the AC.
MMSC	6771	Skip if error flag is a 1.
MMCF	6772	Clear error flag and DT flag.
MMRS	6774	Read status bits into the content of AC 0-7. The bit assignments are: AC0 = DT flag AC1 = Error flag AC2 = End (Selected tape at end point) AC3 = Timing error AC4 = Reverse tape direction AC5 = Go AC6 = Parity or mark channel error AC7 = Select error

CONTROL MODES

The seven modes of operation loaded into the function register during the MMLF command are used as follows:

Move: Initiates movement of the selected transport tape in either direction. Mark channel errors are inhibited in this mode.

Search: As the tape is moved in either direction, sensing a block mark causes both the data flag and the DECtape (DT) flag to rise. The data flag causes a computer data break to deposit the block number in core memory at the address held in MAC. The DT flag initiates a program interrupt to cause the program to jump to a subroutine which is responsible for checking the block numbers by using either the block number stored during this operation or by counting the number of times the DT flag rises.

Read Data: A block of data is read in either direction, the data flag rises to cause a data break each time a 12-bit word is to be transferred, and the DT flag is raised to initiate a program interrupt at the end of the data block. The program is responsible for controlling tape motion at the end of a block transfer and must stop motion or change the contents of the function register when the DT flag rises. The transport continues reading until taken out of the read data mode.

Read All Bits: In this mode of operation the three information channels are continuously read and transferred to the computer. This mode is similar to the read data mode except that the DT flag rises each time the data flag rises. The read all bits mode is used to read an unusual tape format which is not compatible with the read data mode. The DT flag does not cause an interrupt when in this mode.

Write Data: A block of data is written on tape in either direction, the data flag is raised to effect each transfer, and the DT flag is raised at the end of the block as in the read data mode.

Write All Bits: This special mode of operation is used to write information at all positions, disregarding blocks (such as in writing block numbers). The mode is similar to the read all bits mode for writing. The DT flag does not cause an interrupt in this mode.

Write Mark and Timing: This mode is used to write on the timing and mark channels to establish or change block length.

PROGRAMMED OPERATION

Pre-recording of a reel of DECtape, prior to its use for data storage, is accomplished in two passes. During the first pass, the timing and mark channels are placed on the tape. During the second pass, forward and reverse block mark numbers, the standard data pattern, and the automatic parity checks are written. These functions are performed by the DECTOG program. Pre-recording utilizes the write timing and mark channel control mode and a manual switch in